REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

By this Amendment, and without acceding to the outstanding rejection, independent Claims 22, 27, and 34 have been amended for clarity and to include features of now-cancelled dependent Claims 23, 28, and 35. Claim 30 has also been amended to change its dependency to Claim 27. Claims 1-21, 24, 29, and 36 were previously cancelled. Accordingly, Claims 22, 25-27, and 30-34 are pending, with Claims 22, 27, and 34 being independent.

Each of Claims 22, 27, and 34 now clarifies that the switching signal is different from the display data and switches between the positive phase and the negative phase (Claim 22) or controls a switching of a positive phase and a negative phase (Claims 27 and 34). These claims also have been amended to change the term "one specified bit" to "a highest order bit" and to change the term "other bits" to "remaining lower order bits." When converting display data, a highest order bit of the display data is set to logic "0" by a first exclusive logic circuit when the switching signal and the highest order bit match each other and is set to logic "1" by the first exclusive logic circuit when the switching signal and the highest order bit do not match each

other. Each remaining lower order bit of the display data is set to logic "1" by an associated second exclusive logic circuit of a plurality of second exclusive logic circuits when the highest order bit matches the remaining lower order bit and set to logic "0" by the associated second exclusive logic circuit when the highest order bit does not match the remaining lower order bit. The first data and the second data (Claims 27 and 34) or the first display data and the second display data (Claim 22) are in the same bit pattern except for the highest order bit when converting the display data.

The collective disclosures of Kanatani, Sakaguchi, and Lee fail to teach or suggest at least the foregoing features of Applicants' invention.

For example, Lee discloses XNOR logic circuits 240, 244 and XOR logic circuits 242, 246 that each receive as inputs adjacent bits from a 20-bit signal Q"". *See* Lee, Figure 18. However, none of the bits of Lee's 20-bit signal Q"" is a switching signal that differs from display data, as particularly recited in each of Claims 22, 27, and 34. Moreover, though Lee discloses, for example, XNOR gate 240 taking A[0] 232-0 and A[1] 232-1 as inputs and producing a logic value '1' if the two inputs are identical, and XOR gates 242-1 through 242-7 each taking as input adjacent bits

A[1] 232-1 through A[8] 232-8 and producing a logic value '1' if the two input values are not equal, the outputs of Lee's XNOR and XOR gates are input to AND gate 248 to produce a single MATCH signal 222, rather than being output as data for display. Contrast Lee's MATCH signal 222 with Applicants' claimed display data.

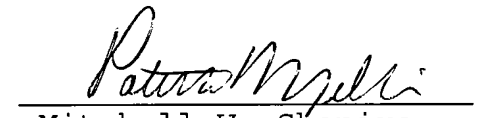
Kanatani and Sakaguchi fail to cure the deficiencies noted above for Lee.

Accordingly, the claims distinguish patentably from the collective disclosures of Kanatani, Sakaguchi, and Lee and are allowable.

A prompt Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10079) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

By: 

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